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LSI Logic Corporation
Legal Department – IP
1621 Barber Lane, MS D-106
Milpitas, CA 95035

Date April 4, 2007

Number of pages including cover sheet 2

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To: US PTO
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TC 2113
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Phone No.
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From: Connie del Castillo
Intellectual Property Paralegal
Telephone (408) 433-7191
No.
Fax No. (408) 433-7460

REMARKS:

Urgent For your review Reply ASAP Please comment

Application Number: 10/706,127
Filing date: November 12, 2003
First named inventor: Maurizio Spadari
Attorney docket number: 03-1868 / 1496.00348

Transmitted herewith for filing via facsimile:

- Status Request Letter

Pursuant to 37 C.F.R. 1.8, I hereby certify that this correspondence is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date indicated below:

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PAGE 1/2 * RCVD AT 4/4/2007 5:45:37 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/5 * DNIS:2738300 * CSID:408 4337460 * DURATION (mm:ss):00:50

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NO. 517

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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APR 04 2007

In re Application of : Maurizio Spadari

Serial No.: 10/706,127

Group Art Unit: 2113

Filed: 11/12/2003

For: Methodology for debugging RTL
simulations of processor based
system on chip

Atty Docket: 1496.00348 / 03-1868

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STATUS REPORT

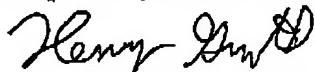
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants request a status of the above referenced application. Please mail the status notification to the address stated below.

LSI Logic Corporation
1621 Barber Lane, MS D-106
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408-433-7475
Date: 4/2/2007

Respectfully submitted,



Henry Groth, Ph: [+1] 408-433-7191

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